18. The data communication system of Claim 12, wherein the reset circuit is a pre-charge circuit.

19. The data communication system of Claim 12, wherein the reset control signal is a pulse signal generated by a pulse generator.

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20. The data communication system as in Claim ~~21~~ 12, wherein the pulse generator is triggered by a signal indicative of the input monitor signal.

21. A method for transferring data in a data communication system for a semiconductor memory system having at least one data path comprising the steps of:

connecting a central data path to the at least one data path at a junction circuit;

receiving data in the junction circuit;

processing the data;

transferring the data out of the junction circuit;

resetting of the junction circuit for preparation for receipt of new data; and

controlling the resetting to prevent resetting while the data is being at least one of received and processed.

22. The method of Claim 21, further including the steps of:

receiving an input monitor signal indicating that the data is being transferred to the junction circuit; and